IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: MBOUOMBOUO, Benjamin et al.

Serial No.: 09/828,553

Filed: April 5, 2001

For: BUFFER CELL INSERTION AND ELECTRONIC DESIGN AUTOMATION

Art Unit: 2825

Examiner: Kik, Phallaka

DECLARATION OF MARK SALVATORE UNDER 37 C.F.R. § 1.132

I, MARK SALVATORE, hereby declare as follows:

1. I have been employed as a paralegal with LSI Logic Corporation since January 2, 2001;

2. The file containing the original invention disclosure that was signed and dated by the inventors for the subject application was lost;

3. It is the custom and practice of LSI Logic Corporation to enter an electronic log entry into the LSI Logic patent database when an invention disclosure is received from inventors employed by LSI Logic Corporation;

4. The attached copy of the electronic log from the LSI

Logic patent database for the subject application indicates that a copy of the invention disclosure for "OPTIMIZED REPEATER INSERTION" attached hereto was received by LSI Logic Corporation before the filing date of February 20, 2001, of U.S. Patent Application US 6,546,541 B1 by Petranovic, et al.;

5. The undersigned further declare that all statements made herein of my own knowledge are true; and that all statements not based on my own knowledge are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

December 1, 2003 /s/ M. L. Salvatore

DATE SIGNATURE

MARK SALVATORE

encl:

(1) copy of invention disclosure for "OPTIMIZED REPEATER INSERTION"

(2) copy of electronic log from the LSI Logic Corporation database

DOCKET NO. 99-253
66254(6653)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Examiner: Kik, Phallaka

DECLARATION UNDER 37 C.F.R. § 1.131

We, BENJAMIN MBOUOMBOUO, STEFAN GRAEF and JUERGEN LAHNER, hereby declare as follows:

1. We are the co-inventors of the invention disclosed and claimed in the subject application;

2. We submitted a copy of the invention disclosure attached hereto for "OPTIMIZED REPEATER INSERTION" to LSI Logic Corporation before the filing date of February 20, 2001, of U.S. Patent Application US 6,546,541 B1 by Petranovic, et al.;

3. The attached excerpt from the LSI Logic Corporation database indicates that the invention disclosure for the subject application was received by LSI Logic Corporation

before the filing date of February 20, 2001, of U.S. Patent Application US 6,546,541 B1 by Petranovic, et al.; and

4. The undersigned further declare that all statements made herein of our own knowledge are true; and that all statements not based on our own knowledge are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

12/02/03
DATE

/s/
SIGNATURE

BENJAMIN MBOUOMBOUO

DATE

/s/
SIGNATURE

STEFAN GRAEF

12/01/03
DATE

/s/
SIGNATURE

JUERGEN LAHNER

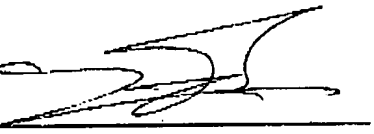
before the filing date of February 20, 2001, of U.S. Patent Application US 6,546,541 B1 by Petranovic, et al.; and

4. The undersigned further declare that all statements made herein of our own knowledge are true; and that all statements not based on our own knowledge are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

_____ /s/_____

DATE SIGNATURE

BENJAMIN MBOUOMBOUO

Dec/05/2003 /s/ 

DATE SIGNATURE

STEFAN GRAEF

_____ /s/_____

DATE SIGNATURE

JUERGEN LAHNER

LSI Logic Invention Disclosure Form Disclosure No. 99-253

1. Inventors:

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2. Title of Invention - Optimized Repeater Insertion

3. Conception of invention

a1. Date of first drawing: July 24th, 1999.
b1. Date of first written description: July 24th, 1999
b2. Where is description found: attached.
c1. Date of first oral disclosure: August 11th, 1999
c2. To Whom: Shalini Rubdi

4. Construction of Device: See figure below

5. Test of Device (method)

a. Date: N/A
b. Witness: N/A
c. Result: N/A

Inventors:

_____ Date: _____
_____ Date: _____
_____ Date: _____

Witness, read and understood by:

Print Name: _____ Sign _____ Date _____
Print Name: _____ Sign _____ Date _____

6. Sale

a. Was invention sold? No

7. Use

a. Is invention presently being used? No.

8. Related printed publications, patents, patent application:

None known

9. Was invention

a. Conceived during performance of government contract? No.

b. Constructed during performance of government contract? No.

c. Tested during performance of government contract? No.

d. Contract number: N/A

10. Was invention

a. Conceived during performance of customer contract? No.

b. Constructed during performance of customer contract? No.

c. Tested during performance of customer contract? No.

d. Customer name? N/A

1. General purpose of the invention

The general purpose of this invention is to define the requirements for an optimized repeater insertion to improve path delays in a design. This is only ensured if routing, placement and in-place algorithm take an optimized interconnect resistance and capacitance values into account. A term ' Optimum Interconnect design rule ' was chosen for covering that.

2. Describe old method

In the past, interconnect and cells where treated as two independent entities, therefore making it an option to insert repeaters along long wires.

3. Disadvantages of old method

In deep sub micron technologies it results always in a sub-optimal design when the maximum or non optimized distance between two cells is exceeded. This can and does happen in today's designs.

Inventors:

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4. Describe the invention

The optimized distance is coded in the technology library and can be read by all EDA tools. e.g. during the routing process an "Optimum Interconnect design rule" would force the router to insert a repeater cell after reaching this optimized distance and then go on with its regular routing. This can be used for global net buffering like shown in Fig. 1.

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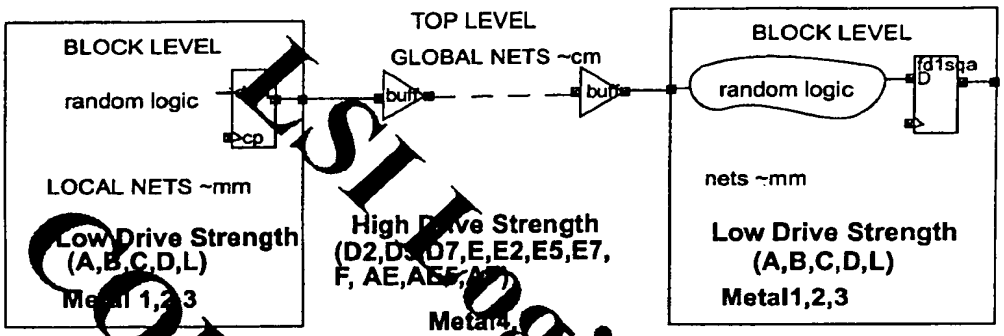

Figure 1: Global net buffering

The usage of an optiomized interconnect resistance and capacitance is not only usable for point to point connections (net with 1 fanout) but also for nets with more than one fanout. In this case, the effective length will be determined and a repeater dropped at the appropriate locations for this net.

5. Give details of operation

During the routing algorithm an estimate of the optimal number of buffers to be inserted for this net has to be done. The Fig. 2 illustrates the function of delay on one path vs. number of buffers. It makes sure that there is always an optimal number of buffers on one path. This

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graph is for one particular interconnect length..

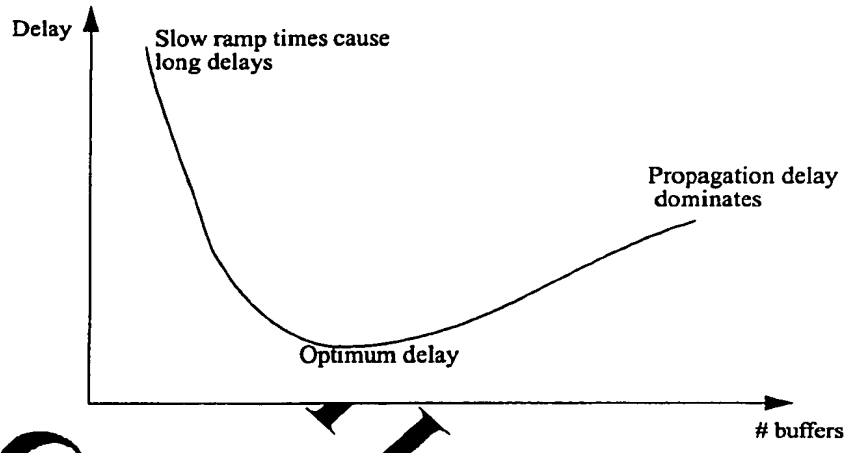

Figure 2: Delay versus buffer graph

If nets, this is especially true for global nets, are longer than the critical net length, buffers have to be inserted. If this isn't done, the ramp times are very slow and therefore the delay very high. The more buffers are inserted, the better the ramp times are and the better the overall delay is. However, this can be only done to a certain extent since the propagation delay of the inserted buffers can dominate with a certain number. Therefore, the number of buffers have to be found, which guarantees the shortest delay and determines the optimum length for repeater insertion.

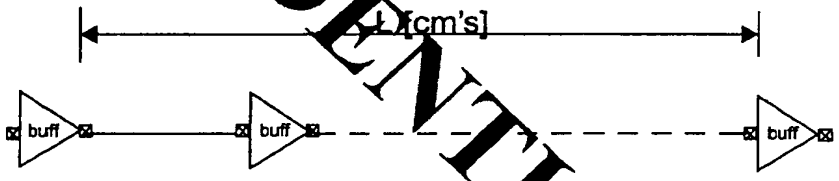

Figure 3: Buffering long nets

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Algorithm for optimized buffer insertion

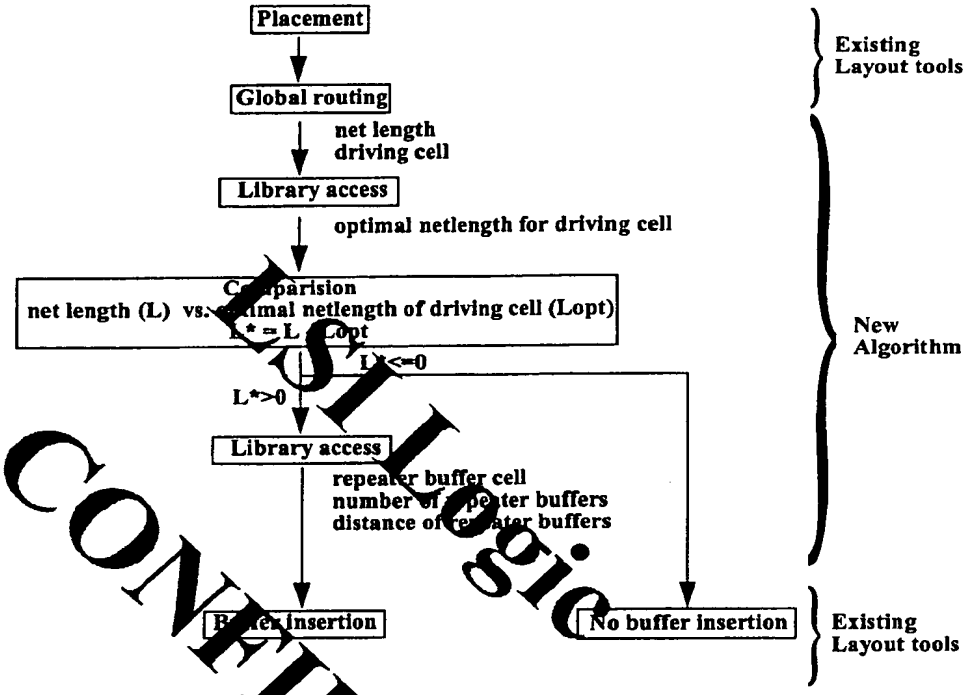

Figure 4: Algorithm for optimized buffer insertion

After placement and global routing is done, "net length" and "driving cell" information will be used for selecting the "optimal net length for driving cell" in a library lookup-table. This value will be compared against the "net length". The following formula will be used for a determination if a buffer insertion has to be done or not: "net length (L)" - "optimal net length for driving cell (Lopt)" =L*. If L* is >0, a buffer insertion has to be done. A second library access will then be done to get the following three values: 1) repeater buffer cell, 2) number of repeater buffers, 3) distance of repeater buffers, which will be forwarded to the layout tool. If L* is <=0, no buffer insertion will follow.

6. Advantages of invention:

Having the' Optimized Interconnect design rule' enables the whole design process to narrow down the otherwise big variance of the delay, caused by interconnect. It has been proven that

Inventors:

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Print Name: _____ Sign _____ Date _____

the delay on a signal path which is caused by wires can vary between 0-96% of the stage delay. This big variance introduces enormous uncertainty in the design flow. This invention is to reduce this variance.

7. Indicate alternative methods

There is no real alternative currently known.

8. If a joint invention, indicate contribution by each inventor:

All inventors contributed equally to this invention.

9. Features believed to be new

Introducing 'Optimized Interconnect design rule' as a design rule is believed to be new.

10. State opinion of relative value: .

Mandatory for deep micron designs and further technologies

11. Enforceability

Yes, because it is present in software

Inventors:

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Witness, read and understood by:

Print Name: _____ Sign _____ Date _____

Print Name: _____ Sign _____ Date _____

LSI Logic Intellectual Property Law Department Memo
Date: Wednesday, March 07, 2001
LSI Docket Number: 99-253 Law Firm Docket Number: 66254

Title : Optimized Repeater Insertion
Subject: Patent 99-253 - 66254 -

Reminder

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Technology Classification : Software

1. Buffer
2. Insertion

- Disclosure - Received from Inventor(s)